CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A programmable logic device (PLD) including a plurality of logic array blocks (LAB's) connected by a PLD routing architecture, wherein at least one LAB includes a logic element (LE) configurable to arithmetically combine a plurality of binary input signals in a plurality of stages, the LE comprising:

look-up table (LUT) logic having K inputs (a "K-LUT"), the K-LUT configured to input the binary input signals at respective inputs of the K-LUT logic cell and to provide, at a plurality of outputs of the K-LUT logic cell, respective binary result signals indicative of at least two of the plurality of stages of the arithmetic combination of binary input signals;

an input line network including a network of input lines, the input lines configurable to receive input signals from the PLD routing architecture that represent the binary input signals and to provide the input signals to the K-LUT; and

an output line network including a network of output lines, the output lines configured to receive, from the K-LUT, output signals that represent the binary result signals and to provide the output signals to the PLD routing architecture.

2. The PLD of claim 1, wherein:

the K-LUT includes a plurality of portions, each portion connected to the routing architecture via the input line network to receive at least some of the input signals; and

each of the plurality of portions of the K-LUT includes circuitry to generate the binary result signals indicative of a respective separate one of the plurality of stages of the arithmetic combination of binary input signals.

3. The PLD of claim 2, wherein:

all of the input signals are provided to each of the plurality of portions of the K-LUT logic cell.

4. The PLD of claim 2, wherein:

the input line network includes at least a first input multiplexer between the routing architecture and a first one of the K-LUT portions and at least a second input multiplexer between the routing architecture and a second one of the K-LUT portions;

the input line network is configured to

in a first state, provide at least a first one of the input signals to both the first K-LUT portion and the second K-LUT portion, via the first input multiplexer and the second input multiplexer, respectively, and

in a second state, instead provide a first carry-in signal to the first K-LUT portion and a second carry-in signal to the second K-LUT portion, via the first input multiplexer and the second input multiplexer, respectively.

5. The PLD of claim 4, wherein:

the K-LUT portions include at least a first K-LUT portion and a second K-LUT portion;

the output line network includes at least a first output multiplexer, controlled by the second one of the input signals, and at least a second output multiplexer, controlled by the second one of the input signals,

the first K-LUT portion is comprised of a first sub-portion and a second sub-portion;

the second K-LUT portion is comprised of a third sub-portion and a fourth sub-portion;

the first output multiplexer selects between the output of the first sub-portion and the second sub-portion; and

the second output multiplexer selects between the output of the third sub-portion and the fourth sub-portion.

6. The PLD of claim 5, wherein:

each of the first K-LUT portion and the second K-LUT portion is a K-1 LUT.

7. The PLD of claim 6, wherein:

each of the first sub-portion, the second sub-portion, the third sub-portion and the fourth sub-portion is a K-2 LUT.

8. The PLD of claim 5, wherein:

the output line network includes at least a third output multiplexer, controlled by the third one of the input signals; and

the third output multiplexer selects between the output of the first output multiplexer and the second output multiplexer.

9. The PLD of claim 2, wherein:

the input line network includes selector circuitry configurable such that,

in a first state, each of a collection of inputs to the K-LUT that includes an input to each of the portions of the K-LUT receive a same particular binary input signal, and

in a second state, at least some of the collection of inputs to the K-LUT do not receive the particular binary input signal.

10. The PLD of claim 9, wherein:

the selector circuitry of the input line network includes a plurality of input multiplexers, the outputs of which are connected to the collection of inputs to the K-LUT, and

the input multiplexers are configurable such that, in the first state, each of the input multiplexers provides the particular binary input signal to the output of that multiplexer and, in the second state, each of at least some of the input multiplexers provides other than the particular binary input signal to the output of that multiplexer.

11. The PLD of claim 8, wherein:

the output line network includes a fourth output multiplexer controlled by the third one of the input signals; and

the fourth output multiplexer selects between the output of the third sub-portion and the fourth sub-portion.

12. The PLD of claim 2, wherein:

the K-LUT portions include at least a first K-LUT portion and a second K-LUT portion;

the first K-LUT portion is comprised of a first sub-portion and a second sub-portion;

the second K-LUT portion is comprised of a third sub-portion and a fourth sub-portion;

the output line network includes a multiplexer configurable to selectively provide an output from one of the third sub-portion and the fourth sub-portion, based on signal indicative of a signal output from the second sub-portion.

13. The PLD of claim 12, wherein the signal output from the second sub-portion is indicative of a carry-out of the first stage.

14. The PLD of claim 1, further comprising:

at least one output multiplexer, each of the at least one output multiplexers coupled to select among signals at the outputs of the K-LUT logic cell, under the control of a carry-in signal to the LE, to provide an arithmetic output signal from the LE to an output line of the output line network.

15. A programmable logic device (PLD) including a plurality of logic array blocks (LAB's) connected by a PLD routing architecture, wherein at least one LAB includes a logic element (LE) configurable to arithmetically combine a plurality of binary input signals in a plurality of stages, the LE comprising:

look-up table (LUT) logic having K inputs (a "K-LUT"), the K-LUT configured to input the binary input signals at respective inputs of the K-LUT logic cell and to provide, at a plurality of outputs of the K-LUT logic cell, respective binary result signals indicative of the arithmetic combination of binary input signals;

an input line network including a network of input lines, the input lines configurable to receive input signals from the PLD routing architecture that represent the binary input signals and to provide the input signals to the K-LUT;

an output line network including a network of output lines, the output lines configured to receive, from the K-LUT, output signals that represent the binary result signals and to provide the output signals to the PLD routing architecture; and

at least one output multiplexer, each of the at least one output multiplexers coupled to select among signals at the outputs of the K-LUT logic cell, under the control of a carry-in signal to the LE, to provide an arithmetic output signal from the LE to an output line of the output line network.